ADDITIONAL FEE:

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R E M A R K S

The Office Action issued December 14, 2001 has been received and its contents have been carefully considered.

Claims 1-5 have been thoroughly reviewed and amended to more clearly delineate the invention as required by 35 USC §112. Claim 2 has been canceled and the subject matter thereof has been incorporated into claim 1. Claim 1 is the only independent claim in this application.

Claims 1 and 3-5 (all of the pending claims in this application) stand rejected under 35 USC §103(a) as being unpatentable over two U.S. patents to Pechanek (Patents Nos. 5,640,586 and 5,682,544). This rejection is respectfully traversed for the reasons given below.

The Pechanek processors were primarily developed for matrices calculations as they were needed to model complex neural networks. Although the nature of a computer is to perform a plurality of tasks, the intention was for large

mathematical calculations by the use of an SIMD processor connected to a host computer. Looking at the Pechanek patent '544, the drawing sheet 8/11 shows that the Processor Elements (PE) are connected to a Root Tree Processor which is controlled by data provided from the host computer. The host computer provides instructions and data required to solve the problem at hand. In contrast, the present invention concerns a self-contained computer with the instructions stored either in internal or external memory so the processor can operate independently of other processors.

The computer according to the present invention can be connected to another processor via an external interface, but this is not required. The present invention was developed to provide a processor that can have its hardware initially designed. Thereafter, a programmer writes instructions to determine the data paths of the processor, whereas traditional processors already have their basic sets of instructions already defined. Therefore, with the help of an experienced programmer in the use of the present invention, the system potential would increase as the programming techniques are enhanced. Also by the use of multiple components, multiple instructions can be operating

at the same time. The way this is done can be programmed by the programmer and need not be designed at the hardware stage. The intention of the present invention was to design a basic system with as much power as required by the user, by the use of more memory and more processing components, which are then programmed for operation in a desired way by the programmer.

Page 10, lines 11 to 31, of the specification explains the procedures which are needed to operate the computer when turned on, and would normally be installed by the computer supplier. The main set of instructions are used to operate the operating system (e.g., Microsoft Windows). From this point additional procedures can be created that provide a custom function as mentioned in the specification. In contrast, the Pechanek system has a predefined set of instructions which are called up by a transfer of data from the host computer.

As noted by the Examiner, the Pechanek system does have complex data paths which comprise a number of Processor Elements (PE's) where each PE can be connected in a grid with the use of ALU's with bypass switches. The key difference is that the present invention cannot perform any

computational calculations on a grid axis and uses the grid only to route data to the various computing components (ALU's, registers, input/output circuits, memory and cache memory, etc.). The Pechanek processor PE can just allow data to pass without processing. If all PE's in the Pechanek processor only allow a passing of data, then no calculations can be performed and the system is no longer a computer, whereas the present invention grid only directs the information to a desirable computing component. Therefore, although both systems mention the term grid, they still operate differently. The present system cannot perform the same data paths as the Pechanek system and vice-versa.

Pechanek developed a Single Instruction Multiple Data processor (SIMD) although the present processor shows only one Instruction Set Decoder (ISD) and for simplicity the processor has been designed as an SIMD. But the advantage of the instant system is its simplicity in concept. You could have a single chip with two or more IDS units so that two programs can operate on the same processor using the same memory and Processing Components. It is obvious that two or more programs would be running at the same time on

the processor and there would be the need to ensure that no two Processing Components conflict with each other (as shown in Figure 9 and mentioned on page 12, lines 5-10 of the specification). Also, because there are multiple data paths, a competent programmer could program the Instruction Set Decoder to pipeline instructions by being able to use the multiple ALU's, registers and multiple data paths at once so that the look-ahead feature of pipelining could be taken into account. This is where the intention of the processor becomes relevant by allowing the processor to process multiple instructions on a single instruction or multiple instructions. Therefore, the processor can be either SIMD or Multiple Instruction Multiple Data Path (MIMD), whereas Pechanek is limited to SIMD.

The present invention provides that the interconnections on the grid are made to a plurality of components, not that there are a plurality of components on the interconnections of the grid. Although the switch does contain components such as bi-directional data switches, it does not contain Processing Elements as found in Pechanek and the Illiac IV processor. The switch at each node is an elementary component, only used to route data. The

processing with the present invention occurs on the Processing Components which are not on the interconnections.

Claim 1, as amended, now defines a microprocessor wherein a plurality of components are connected on a grid "and wherein each of said plurality of components can be switched under program control to be connected to a predetermined selection of one or more of said plurality of components to route data through said grid for processing by said [selected] plurality of components." In so doing, the program control serves to interconnect selected ones of the plurality of components, using the grid to route the data between them for processing. As explained above, this arrangement is neither taught nor suggested by the Pechanek patents.

Accordingly, it is believed that claims 1 and 3-5, as now amended, distinguish patentably over the Pechanek patents. This application is therefore believed to be in condition for immediate allowance. A formal Notice of Allowance is accordingly respectfully solicited.

Respectfully submitted,

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